WHAT IS CLAIMED IS:

1. An increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising:

a delay circuit block operable to receive and align at least a block of said debug data;

a first mask circuit connected to said delay circuit block, wherein said first mask circuit is operable to select a first portion of said block of aligned debug data for incrementing;

a second mask circuit connected to said delay circuit block, wherein said second mask circuit is operable to select a second portion of said block of aligned debug data for decrementing; and

an accumulation circuit connected to said first mask circuit and said second mask circuit, said accumulation circuit for generating an accumulated value based on outputs provided by said first and second mask circuits.

2. The increment/decrement circuit as recited in claim 1, wherein said block of said debug data comprises 16 bits.

3. The increment/decrement circuit as recited in claim 1, wherein said block of said debug data forms a portion of an 80-bit wide debug data signal.

4. The increment/decrement circuit as recited in claim 1, wherein said delay circuit block is operable responsive to a delay_values signal that provides clock delaying values for each bit in said block of said debug data.

5. The increment/decrement circuit as recited in claim 1, wherein said delay circuit block includes a series of registers operable to be tapped for providing a plurality of inputs to a Multiplexer (MUX) block that is controlled by a delay_values signal.

6. The increment/decrement circuit as recited in claim 1, wherein said first mask circuit comprises an AND block having a plurality of 2-input AND gates for bit-wise ANDing said block of said debug data with a multi-bit inc_mask signal.

7. The increment/decrement circuit as recited in claim 1, wherein said first mask circuit comprises:

an XOR block having a plurality of XOR gates for bit-wise XORing said block of said debug data with a multi-bit inc_invert signal to generate a multi-bit output signal; and

an AND block having a plurality of 2-input AND gates for bit-wise ANDing said multi-bit output signal with a multi-bit inc_mask signal.

8. The increment/decrement circuit as recited in claim 1, wherein said accumulation circuit comprises:

a first population count circuit coupled to said first mask circuit;

a second population count circuit coupled to said second mask circuit; and

an adder circuit coupled to said first population count circuit and said second population count circuit.

9. The increment/decrement circuit as recited in claim 1, wherein said accumulation circuit comprises:

a first population count circuit coupled to said first mask circuit;

a second population count circuit coupled to said second mask circuit; and

a subtract circuit coupled to said first population count circuit and said second population count circuit.

10. The increment/decrement circuit as recited in claim 1, wherein said accumulation circuit is operable to forward a signal indicative of an instantaneous outstanding transaction count based on outputs provided by said first and second mask circuits.

11. The increment/decrement circuit as recited in claim 10, wherein said instantaneous outstanding transaction count is forwarded to a counter circuit for further processing.

12. A system for determining latency, comprising:

a first performance counter connected to a bus carrying debug data, said first performance counter being operable to determine a number of instantaneous outstanding transactions;

a second performance counter disposed in communication with said first performance counter, said second performance counter being operable to determine aggregate latency; and

a third performance counter disposed in communication with said bus, said third performance counter being operable to determine a total number of transactions, whereby average latency is expressed as the ratio of said aggregate latency to said total number of transactions.

13. The system as recited in claim 12, wherein said debug data comprises a 16-bit wide signal.

14. The system as recited in claim 12, wherein said first performance counter comprises a state machine operable to increment and decrement.

15. The system as recited in claim 12, wherein said first performance counter comprises:

a delay circuit block operable to receive and align at least a block of said debug data;

a first mask circuit connected to said delay circuit block, wherein said first mask circuit is operable to select a first portion of said block of aligned debug data for incrementing;

a second mask circuit connected to said delay circuit block, wherein said second mask circuit is operable to select a second portion of said block of aligned debug data for decrementing; and

an accumulation circuit connected to said first mask circuit and said second mask circuit, said accumulation circuit for coupling a value based on outputs provided by said first and second mask circuits.

16. The system as recited in claim 12, wherein said performance counters further comprise a counter circuit that when said counter circuit is enabled, the counter circuit performs an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value.

17. The system as recited in claim 12, further comprising a digital logic component disposed in communication with said second performance counter and said third performance counter, wherein said digital logic component is operable to determine said average latency.

18. A computer system having an increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising:

means for receiving and aligning at least a block of said debug data;

means for selectively asserting an increment signal based on a first portion of said block of aligned debug data;

means for selectively asserting a decrement signal based on a second portion of said block of aligned debug data; and

means for generating an accumulated value based on said increment and decrement signals.

19. The computer system as recited in claim 18, wherein said means for generating an accumulated value is operable to forward a signal indicative of an instantaneous outstanding transaction count based on said increment and decrement signals.

20. The computer system as recited in claim 19, wherein said instantaneous outstanding transaction count is forwarded to a counter circuit for further processing relative to operations selected from the group consisting of latency calculations, advanced triggering, debug calculations, coverage calculations, and performance analysis.